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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/415,060	10/12/1999	TAKASHI YANO	0378-0360P	4255

7590 03/26/2004

BIRCH STEWART KOLASCH & BIRCH LLP
P O BOX 747
FALLS CHURCH, VA 220400747

EXAMINER	
TRAN, NHAN T	

ART UNIT	PAPER NUMBER
2615	6

DATE MAILED: 03/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/415,060	Applicant(s) YANO, TAKASHI	
	Examiner Nhan T. Tran	Art Unit 2615	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 December 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1 & 11 have been considered but are moot in view of the new ground(s) of rejection.

In response to the Applicant's arguments stated in the first paragraph of page 16 that Watanabe fails to teach or suggest the claimed feature of a digitizing circuit for converting an output of the noise reducing circuit to a digital signal in accordance with the first clock, an amount of digital signal being substantially proportional to a ratio of the first clock to a clock outputted from the frequency selector, the Examiner respectfully submits a teaching of Hieda to compensate the silence in Watanabe for controlling the operation of the A/D converter (30).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 5-8, 10-11, 15-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe (US 6,529,236) in view of Hieda (US 6,377,301).

Regarding claim 1, Watanabe discloses a solid state image pickup apparatus comprising:

a mode setting circuit for allowing an operator to select desired one (partial pixel read mode, i.e., ¼ read mode) of plurality of modes (partial read mode, full pixel read mode, isochroous mode, asynchronous mode) matching with a display format of a displays a video signal fed thereto (see Figs. 1A-5; col. 4, lines 24-34 & col. 6, lines 6-23);

a clock generating circuit for generating a plurality of clocks (corresponding to plurality of modes) including a first clock (e.g., clock for driving ¼ read pixel mode) and a second clock (e.g., clock for driving full pixel read mode) higher in frequency than the first clock (see Figs. 3 & 5; col. 4, lines 25-34). It should be noted that the clock for driving the full pixel read mode in Fig. 3 must be faster than the clock for driving the ¼ pixel read mode in Fig. 5 since the full mode requires two fields to read out all pixels for interlace while the ¼ read mode skips reading out some pixels and reads one frame at a time which requires a slower clock for reading and transferring compared to the full mode.

a frequency selector (CCD drive control 28) for selecting either one of a first clock and a second clock in accordance with a mode fed from the mode setting circuit (see Figs. 1A; col. 3, lines 6-10 and col. 5, lines 3-12 wherein, in order for the system function properly, CCD drive control selects an appropriate synchronous clock, timing pulses to drive the CCD and the signal processing 28 for each pixel read mode);

an image pickup section (22) including a plurality of photosensitive cells for transforming, by photoelectric transduction, light incident thereto from a scene to be picked up, the image pickup section picking up the scene and producing signal charges representative of the scene in accordance with an output of frequency selector (see Figs 1A, B, 3-5; col. 4, lines 4-33);

a noise reducing circuit (28) for reducing noise components included in a signal output from the image pickup section (see Fig. 1A; col. 5, lines 14-19);

a digitizing circuit (30) for converting an output of the noise reducing circuit to a digital signal in accordance with the first clock (see Fig. 1A; col. 5, lines 26-42 wherein the first clock is selected by the CCD drive control 28 in accordance with selected pixel read mode as analyzed above);

a signal processing circuit (32) for processing an output of the digitizing circuit in a manner matching with picture display (see Fig. 1A; col. 6, lines 6-23);

a controller (CPU 26) for controlling the clock generating circuit, the frequency selector, the image pickup section, the noise reducing circuit, the digitizing circuit and the signal processing (see Figs. 1A-B wherein all processes in the camera is controlled by the Central Processing Unit 26);

wherein the plurality of modes include a first mode (i.e., ¼ pixel read mode) in which the frequency selector outputs the first clock (for driving ¼ pixel read mode) and second mode (i.e., full pixel read mode) in which the frequency selector outputs the second clock (for driving full pixel read mode). See Figs. 3-5 for the read modes of the CCD wherein each mode is driven by its corresponding clock in order for the CCD to function properly.

Watanabe is silent about how the ADC 28 to be controlled so that an amount of digital signal (on line 108) being substantially proportional to a ratio of the first clock (on line 100) to a clock (on line 124) outputted from the frequency selector as shown in Fig. 1A. However, it should be noted that a ratio of the first clock to a clock for controlling the signal processing 28 inherently exists since the signal processing 28 performs sampling, holding, filtering, etc. (col. 5,

lines 12-25) that must require a synchronous clock at a specific ratio with respect to the first clock for driving the CCD so that the operations of the CCD and the signal processing circuit are synchronized at a certain timing period to avoid mismatching between the operations.

Furthermore, Hieda teaches that the operations of a CCD (1), sample and hold circuit (8) and A/D converter (9) are driven at a certain clock generated by the oscillator (5) and/or frequency divider circuit (6) (see Fig. 1; col. 4, lines 27-29). According to Fig. 1, it is clear that the output of A/D converter is always maintained substantially proportional to a ratio of the CCD clock to a clock output from driving circuit (2) to drive the sample and hold circuit (at least at a ratio 1:1) since the driving clocks of the above units are derived from only one frequency oscillator (5) as a source.

It would ensure synchronous operations without mismatching among the CCD, sample and hold circuit and the A/D converter by supplying these units with corresponding clocks that are derived from one source of operating frequency.

Therefore, it would have been obvious to one of ordinary skill in the art to configure the operations of the CCD (22), signal processing circuit (28) and the ADC (30) in Watanabe in view of the teaching of Hieda by enabling the above units to operate in response to the driving clocks derived from one source of driving frequency so that the operations of the imaging device would be maintained at a high accuracy wherein the an amount of the digital output from the A/D converter would be always substantially proportional to a ratio of the first clock to a clock outputted from the CCD drive control circuit.

Regarding claim 5, Watanabe discloses vertical transfer path VCCD and horizontal transfer path HCCD in which the drive signal (100) of the first clock for driving ¼ pixel read mode is fed to the transfer paths of the image pickup section (22). A resetting device must be included either in VCDD or HCCD or both in order for a control signal (on line 100) to drive the VCCD and HCCD to reset (discharge) signal charges detected on the transfer paths after transferring mixed signals in one frame in order to receive subsequent signal charges for the next frame (see Fig. 5; col. 4, lines 55-63).

Regarding claim 6, Watanabe discloses a fourth mode (camera record mode as shown in Figs. 10 & 11) in which the output (line 100) to be fed to the resetting device (in VCCD or HCCD) comprises the first clock (clock for driving ¼ read mode) while an output of the frequency selector comprises the second clock (clock for driving full read mode). It is noted that the second clock is selected when the user releases command for capturing an image to a memory (14) through operation member while the first clock maintains for displaying real time images on the display (also see col. 14, line 61 – col. 15, line 31). With respect to a "third mode", it is disclosed by Watanabe as a display mode for real time image display utilizing only the first clock of ¼ read mode for both driving and resetting control.

Regarding claim 7, as shown in Figs. 3-5, it is clear that the clocks for driving full read mode and ¼ read mode must be in integral ratio to each other (i.e., 4 or ¼).

Regarding claim 8, Watanabe discloses VCCD and HCCD for transferring signal charges output from photosensitive device (PD) in direction of columns and rows, respectively, under control of CPU (see Figs. 3-5; col. 4, lines 35-67).

Regarding claim 10, the signal processing circuit (32) includes a video outputting (112, 36) for feeding a processed signal to the display (see Figs. 1A & B; col. 6, lines 6-23).

Regarding claim 11, the claimed limitations are analyzed with respect to claim 1.

Regarding claim 15, the claimed limitations are analyzed with respect to claim 5.

Regarding claim 16, the claimed limitations are analyzed with respect to claim 6.

Regarding claim 17, the claimed limitations are analyzed with respect to claim 7.

Regarding claim 18, the claimed limitations are analyzed with respect to claim 10.

3. Claims 2 – 4 & 12 – 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe and Hieda as applied to claims 1 & 11 and in further view of Takahashi (JP 06-141330).

Regarding claim 2, Watanabe discloses the processing circuit (28) further clamps image signal at preselected level, and subjects the claimed image signal to white balance adjustment, color correction, tonality correction, and so forth. The combination of Watanabe and Hieda does not expressly teach a color separating circuit for separating a signal output via color filters included in the image pickup section color by color; a frequency band limiting circuit for limiting a frequency band of each output of the color separating circuit; and multiplexing circuit for multiplexing outputs of the frequency band limiting circuit; wherein the color separating circuit, the frequency band limiting circuit and the multiplexing circuit are arranged between the noise reducing circuit and the digitizing circuit. However, as taught by Takahishi, a color separating circuit for separating color signal output from CDS circuit into each color signal R, G and B, and each color signal is inputted to low pass filters (5-7), in which the signal is amplified and only a valid signal of video signal band is extracted with the filter having a lower cut-off frequency than the frequency of a half of the sampling frequency, and further the resulting signal is synthesized/multiplexed into a serial signal by circuit (11) for reducing distortion attended with sampling process at A/D conversion (see Abstract & Fig. 2).

Therefore, it would have been obvious to one of ordinary skill in the art to modify the the combination of Watanabe and Hieda with Takahishi by including a color separating circuit, frequency band limiting circuit and multiplexing circuit to be arranged between the noise reducing circuit and A/D converter for reducing reflection distortion attended with sampling at A/D conversion so that picture deterioration would be prevented.

Regarding claim 3, Takahashi discloses that the low pass filters (5-7) in which only valid signal of the video signal band is extracted with the filter having a lower cut-off frequency than the frequency of a half of the sampling frequency (see Constitution).

Regarding claim 4, Takahishi also discloses an analog adding circuit (11) for adding (synthesizing) the resulting color signal output from each low pass filter corresponding to a particular color as shown in Fig. 2 & Constitution.

Regarding claim 12, the claimed limitations are analyzed with respect to claim 2.

Regarding claim 13, the claimed limitations are analyzed with respect to claim 3.

Regarding claim 14, the claimed limitations are analyzed with respect to claim 4.

4. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe '236 and Hieda as applied to claim 1 and in further view of Watanabe (US 6,522,356).

Regarding claim 9, Watanabe '236 and Hieda do not teach that the photosensitive devices have geometric centers shifted from each other by a distance corresponding to one half of a pitch of the plurality of photosensitive devices in a direction of rows. Watanabe '356 teaches a well-known configuration for an image pickup section that has the pixels disposed in even-number rows being shifted by one half of a pitch in direction of rows from corresponding

pixels disposed in odd-number rows thereby obtaining a well-balanced color resolution of the image pickup section (see Figs. col. 3, lines 21-26; col. 4, lines 44-45).

Therefore, it would have been obvious to one of ordinary skill in the art to further modify the combination of Watanabe '236 and Hieda with Watanabe '356 by reconfiguring the image pickup section in a well-known fashion in which nearby ones of the plurality of photosensitive devices have geometric shifted from each other by a distance corresponding to one half of a pitch of the plurality of photosensitive devices in a direction of rows to obtain a well-balanced color resolution of the image pickup section.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nhan T. Tran whose telephone number is (703) 605-4246. The examiner can normally be reached on Monday - Thursday, 8:00am - 6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Andrew B Christensen can be reached on (703) 308-9644. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NT.

ANDREW CHRISTENSEN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600